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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,615	01/04/2002	Robert F. Wallace	SDK1P007/SDK0296.000US	2529

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,615	WALLACE, ROBERT F.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,12,13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,12,13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,366,933 to Golwalkar et al. in view of US Patent No. 5,172,213 to Zimmerman.

Regarding claim 1, Golwalkar et al. (figure 15) teach a molded semiconductor device package comprising:

a die attach pad (25);

a first (50) and second (90) semiconductor die, each die having a die bond pad (a portion of die bond pad forms on the chip), each of the die positioned such that the die bond pads of each die face in opposite directions, the first (50) and second (90) die being connected to opposing surfaces of the die attach pad (25);

a plurality of contact leads (44, 46) positioned proximate to the first (50) and second (90) die;

a first bonding wire (an upper wire) that is stitch bonded to the die bond pad (a portion of die bond pad forms on the first chip [50]) of the first die (50) and stitch bonded to a first one of the contact leads;

a second bonding wire (a lower wire) that is stitch bonded to the die bond pad (a portion of die bond pad forms on the second chip [90]) of the second die (90) and stitch bonded to a second one of the contact leads; and

a plastic molding cap (60) that encapsulates the first (50) and second (90) die, the first and second bonding wire (upper wire and lower wire), and a portion of the contact leads (44, 46); and

a plastic molding cap (60) that encapsulated the first (50) and second (90) die, the first and second bonding wire (upper wire and lower wire), and a portion of the contact leads (44, 46).

Golwalkar et al. differ from the claimed invention by not showing the plastic molding encapsulates the aluminum wires. However, Zimmerman (figures 1-2) teaches the plastic molding (22) (column 5, lines 21-22) that encapsulates the aluminum wire (20) (column 3, lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Zimmerman into the device taught by Han et al. because it provides interconnection between the elements of the device. The combined device shows a plastic molding cap that encapsulates the first and second aluminum bonding wire.

Golwalkar et al. and Zimmerman further differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 16, Golwalkar et al. (figure 15) teach a molded semiconductor device package comprising:

a die attach pad (25);

a first (50) and a second (90) semiconductor die, each die having a die bond pad (a portion of die bond pad forms on the chip), each of the die positioned such that the die bond pads of each die face in opposite directions, the first (50) and second (90) die being connected to opposing surfaces of the die attach pad (25);

a contact lead (44 or 46) positioned proximate to the first (50) and second (90) die;

a first bonding wire (an upper wire) that is stitch bonded to the contact lead (44 or 46) and stitch bonded to the die bond pad (a portion of die bond pad forms on the first chip [50]) of the first die (50);

a second bonding wire (a lower wire) that is stitch bonded to the contact lead (44 or 46) and stitch bonded to the die bond pad (a portion of die bond pad forms on the second chip [90]) of the second (90) die; and

a plastic molding cap (60) that encapsulated the first (50) and second (90) die, the first and second bonding wire (upper and lower wire), and a portion of the contact lead (44 or 46).

Golwalkar et al. differ from the claimed invention by not showing the plastic molding encapsulates the aluminum wires. However, Zimmerman (figures 1-2) teaches the plastic molding (22) (column 5, lines 21-22) that encapsulates the aluminum wire (20) (column 3, lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Zimmerman into the device taught by Han et al. because it provides interconnection between the elements of the device. The combined

device shows a plastic molding cap that encapsulates the first and second aluminum bonding wire.

Regarding claim 18, Golwalkar et al., and Zimmerman differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 19, the combined device shows the first die contains integrated circuit components configured to form a memory (Golwalkar et al.; column 10, lines 11-12).

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al. in view of Zimmerman, and further in view of US Patent No. 5,735,030 to Orcutt.

Regarding claim 2, the disclosures of Golwalkar et al. and Zimmerman are discussed as applied to claim 1 above.

The combined device differs from the claimed invention by not showing a first conductive ball formation that is formed between the first bonding wire and the die bond pad of the first die; and a second conductive ball formation that is formed between the second bonding wire and the die bond pad of the second die. However, Orcutt (figure 3) teaches a conductive ball formation (21) that is formed between the bonding wire (1) and the die bond pad (5) of the die (7). It would have been obvious to one having ordinary skill in the art at the time the invention was

made to incorporate the teaching of Orcutt into the device taught by Golwalkar et al. and Zimmerman because it is desirable securely to hold the wire on the chip. The combined device shows a first conductive ball formation that is formed between the first bonding wire and the die bond pad of the first die; and a second conductive ball formation that is formed between the second bonding wire and the die bond pad of the second die.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al. in view of Zimmerman, and further in view of US Patent No. 6,437,429 to Su et al.

Regarding claim 6, the disclosures of Golwalkar et al. and Zimmerman are discussed as applied to claim 1 above.

The combined device differs from the claimed invention by not showing the package is either a thin small outline package or a quad flat pack package. However, Su et al. teach the package is a thin small outline package or a quad flat pack package (column 1, lines 13-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Su et al. into the device taught by Golwalkar et al. and Zimmerman, since it is a conventional semiconductor device package.

5. Claims 12, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,366,933 to Golwalkar et al. in view of US Patent No. 5,735,030 to Orcutt and US Patent No. 5,172,213 to Zimmerman.

Regarding claim 12, Golwalkar et al. (figure 15) teach a molded semiconductor device package comprising:

a pair of semiconductor die (50, 90) that are oriented such that a top surface of each die are facing in opposite directions, the top surface of each die having at least one die bond pad (portion of die bond pads form on the semiconductor die [50], [90]);

at least one contact lead (44, 46) positioned proximate to the pair of semiconductor dice (850, 90);

a plastic molding cap (60) that encapsulated the pair of semiconductor die (50, 90), the bonding wire (upper and lower wire) and a portion of the contact lead (44, 46).

Golwalkar et al. differ from the claimed invention by not showing a conductive ball formation positioned on the die bond pad of each die and at least one bonding wire that is stitch bonded to the contact lead and stitch bonded to one of the conductive ball formations on the die bond pad. However, Orcutt (figure 1) teaches a conductive ball (21) formation that is formed on the die pad (5) and the bonding wire (1) is also stitch bonded to the contact lead (9) and stitch bonded to the conductive ball formation (21) on the die bond pad (5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Orcutt into the device taught by Golwalkar et al. because it is desirable securely to hold the wire on the chip and the lead. The combined device shows a conductive ball formation positioned on the die bond pad of each die and at least one bonding wire that is stitch bonded to the contact lead and stitch bonded to one of the conductive ball formations on the die bond pad.

Golwalkar et al. and Orcutt further differ from the claimed invention by not showing the plastic molding encapsulates the aluminum wire. However, Zimmerman (figures 1-2) teaches the plastic molding (22) (column 5, lines 21-22) that encapsulates the aluminum wire (20)

(column 3, lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Zimmerman into the device taught by Golwalkar et al. because it provides interconnection between the elements of device. The combined device shows a plastic molding cap that encapsulated the conductive ball formation and the aluminum bonding wire.

Regarding claim 13, the combined device shows a die attach pad (Golwalkar et al.; 25) that is attached to and sandwiched between the pair of semiconductor die (Golwalkar et al.; 50, 90).

Regarding claim 15, Golwalkar et al., Orcutt and Zimmerman differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al. in view of Zimmerman, and further in view of US Patent No. 6,437,429 to Su et al.

Regarding claim 17, the disclosures of Golwalkar et al. and Zimmerman are discussed as applied to claims 16, 18 and 19 above.

The combined device differs from the claimed invention by not showing the package is either a thin small outline package or a quad flat pack package. However, Su et al. teach the

package is a thin small outline package or a quad flat pack package (column 1, lines 13-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Su et al. into the device taught by Golwalkar et al. and Zimmerman, since it is a conventional semiconductor device package.

Response to Arguments

Applicant's arguments with respect to claims 1, 2, 6, 12, 13 and 15-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
August 18, 2004

DONGHEE KANG
PRIMARY EXAMINER